EE/EET 2240

Tentative Schedule – Summer 2018

Date	Topic(s)	Related Text Sections
May 14	Introduction	1.1 – 2.3
May 15	Kirchhoff's Laws, Power Calculations	3.1 – 3.3
May 16	Resistors, Ohm's Law and Passive Sign Convention	2.4, 3.7
May 17	Simple Circuits	3.4 – 3.6, 3.8
May 18	Dependent Sources	2.3
May 21	Nodal Analysis	4.1
May 22	Nodal Analysis (continued), Mesh Analysis	4.2, 4.3
May 23	Mesh Analysis (continued)	4.4
May 24	Review	
May 25	**Exam #1**	
May 28	**Memorial Day Holiday**	
May 29	PSpice & Computer-Aided DC Circuit Analysis	4.6, Appendices 2,4,6
May 30	Linearity and Superposition	5.1
May 31	Thévenin/Norton Theorems, Maximum Power Transfer	5.2 – 5.4
June 01	Operational Amplifiers	6.1 – 6.3
June 04	Operational Amplifier Circuits	7.5
June 05	Analog Computers	Class Notes
June 06	Capacitors and Inductors	7.1 – 7.2
June 07	Review	
June 08	**Exam #2**	
June 11	Capacitors and Inductors (continued)	7.3
June 12	First-Order Transient Circuit Analysis	7.4, 8.1 – 8.8
June 13	Transient Circuit Analysis with PSpice	Appendix 4
June 14	First-Order Transient Circuit Analysis (continued)	8.1 – 8.8
June 15	Second-Order Transient Circuit Analysis	9.1 – 9.7
June 18	Second-Order Transient Circuit Analysis (continued)	9.1 – 9.7
June 19	Transient Circuit Analysis with PSpice	Appendix 4
June 20	Second-Order Transient Circuit Analysis (continued)	9.1 – 9.7
June 21	Review	
June 22	**Final Exam**	

Actual classroom discussion may vary slightly from this schedule.

Class normally meets Monday through Friday, 8:00AM – 9:15AM,
in LIBR B32 (Pocatello) and CHE 314 (Idaho Falls).

Exams will be in LIBR B32 (Pocatello) and TAB 115 (Idaho Falls Testing Center).